EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 01084671
PUBLICATION DATE : 29-03-89

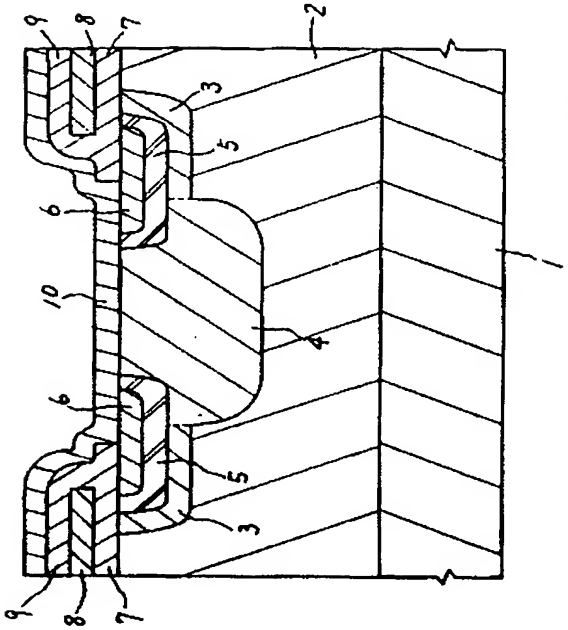
APPLICATION DATE : 28-09-87
APPLICATION NUMBER : 62240769

APPLICANT : HITACHI LTD;

INVENTOR : WATANABE TOKUO;

INT.CL. : H01L 29/78 H01L 29/68

TITLE : SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To decrease an on-resistance and restrain a latch-up by a method wherein a region which is lower than a source in an impurity concentration and the same conductivity type as the source is made sandwiched in between the source and a well of a transistor.

CONSTITUTION: A low concentrated impurity source region is made interposed between an N^+-type source region 6 and a P-type well region 3 of an upright power MOS field effect transistor. By this process, a parasitic bipolar transistor composed of a source, a well, and a drain which serve as an emitter, a base, and a collector respectively is made to decrease in an emitter injection efficiency and also in an emitter ground current amplification factor. A short-circuit resistance between a source and a drain is made to increase, and a channel width per unit area is made larger, so that an on-resistance can be decreased.

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Patent Abstracts of Japan

PUBLICATION NUMBER : 62150770
PUBLICATION DATE : 04-07-87

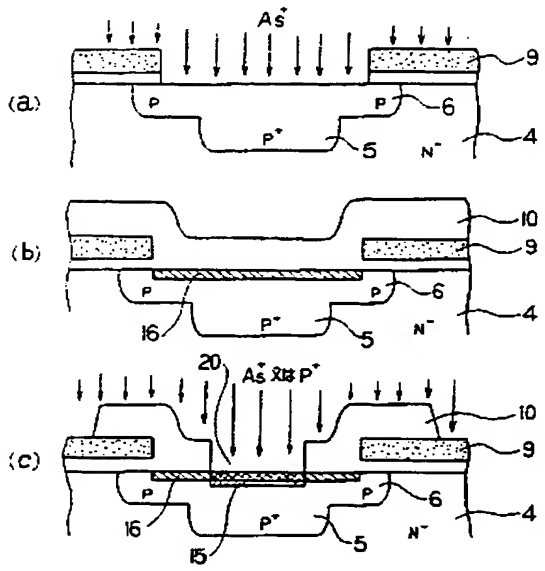
APPLICATION DATE : 24-12-85
APPLICATION NUMBER : 60295146

APPLICANT : FUJI ELECTRIC CO LTD;

INVENTOR : UENO KATSUNORI;

INT.CL. : H01L 29/68 H01L 29/52 H01L 29/78

TITLE : VERTICAL TYPE MOSFET



ABSTRACT : PURPOSE: To increase the maximum working current by suppressing the latch-up phenomenon caused by a parasitic thyristor by a method wherein a source region is composed of two resistance layers of a high impurity density layer and a layer having the impurity density lower than that of the above-mentioned layer, and these two resistance layers are formed on the source region in series.

CONSTITUTION: After a P^+ layer 5 and a P base layer 6 have been formed in an N^- base layer 4, and a gate polysilicon layer 9 has been formed on the N^- base layer 4, the arsenic to be used for a resistance layer 16 is implanted by applying self-alignment using the gate polysilicon layer 9. Then, a CVD (chemical vapor deposition) film 10 to be used for insulation is provided on the whole surface, the CVD film on the part 20 to be metallic contacted is etched by performing a photolithographic process, a high density of arsenic for contact is implanted on the above-mentioned part 20, and a resistance layer 15 is formed. Then, an electrode is formed by performing an annealing and a vapor-deposition of metal. As the resistance value of the resistance layer 16 is controlled accurately by adjusting the quantity of implantation of impurities, the resistance value can be freely selected in accordance with the characteristics of an element.